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FPGA based multichannel PWM controller with embedded dead time

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Abstract: In nowadays industry the voltage source inverters with MOSFET or IGBT devices are used more and more frequently. Such applications include full H-bridge power stages which are prone to shoot through if not properly driven. This situation emerges when the upper and the lower switch from the same side of the bridge are both in on state for some time. The ensuing effect can generate unwanted losses or cause thermal runaway and the result will be a failure of the power switch and even of the whole inverter. A possible solution to the problem is proposed in the paper that injects the so called "interlock delay time" or a "dead time" into the control algorithm. This is made possible with the aid of a programmable logic device which inherent ability for parallel algorithm execution permits to implement multiple Pulse Width Modulator (PWM) devices on a single chip. Because of the physical specifics of the different power transistors the dead time duration can be easily configured via parameters. Moreover the PWM resolution can be easily configured to a non-trivial value such as 9 or 13 bits upon design requirements. All of the above said shows that programmable logic devices outperform the capabilities of most if not any conventional microcontroller available on the market. The proposed algorithm can be used for both soft- or hard-chopping switching strategies. It is highly suitable for industrial applications such as multi-axis robots, that require several driving channels to run simultaneously.

Keywords: Pulse Width Modulation, Dead-time Control, Programmable Logic Device, Commutation Strategy.

I. INTRODUCTION

For driving motors or other loads that may require current reversal full H-bridge power schemes are widely adopted. Their design can differ in both power switches and topology. Various switching components are used for that purpose such as SCRs (Silicon-Controlled Rectifiers) or BJTs (Bipolar Junction Transistors) but at present the MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated-Gate Bipolar Transistors) are the most common ones. The different ways of connecting switches determine the different topologies - half- or full-bridge; single, three-phase or multiphase etc [1, 13, 20, 21, 22]. In addition, the power circuits differ with respect to the selected switching method. The whole variety of topologies and control strategies is beyond the scope of this work. Below is discussed a PWM algorithm and it is proposed a hardware device implementation that can be applied for controlling a full H-bridge of the type shown in Fig. 1.

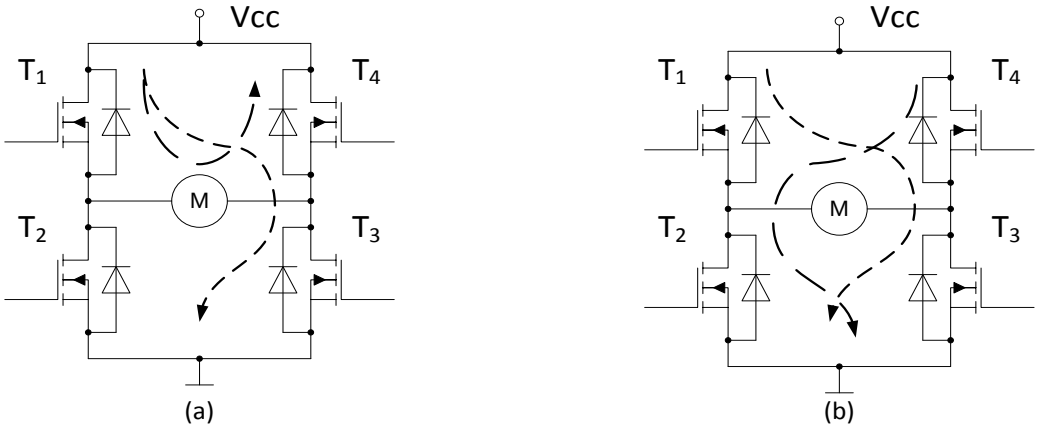

Fig. 1. H-bridge inverter topology and switching strategies for soft-chopping (a) and hard-chopping (b) modes

In the H-bridge N-channel MOSFET transistors are used as power switches. They are controlled by voltage pulses and have very low (in the order of a few milliohms) internal resistance in on-state, which determines the low active power that they dissipate. Since the motor windings are inductive in nature, usually MOSFETs include a flyback diode connected in parallel to its gate and source terminals. Two basic control strategies can be implemented with this circuit – namely soft-chopping mode (Fig. 1, a) and hard-chopping mode (Fig. 1, b) [12].

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In soft-chopping mode, two of the transistors (T2 and T4 for example) are permanently cut-off while T1 is turned on for the entire phase excitation period. The diametrically opposed transistor T3 is controlled by the PWM pulses. When T3 is cut-off, due to the energy stored in the winding, a voltage with reverse polarity is created that attempts to maintain the value of the current flowing therein. In this case the current loop is closed through T1 and the flyback diode of T4. Because in turn-off state of the transistors the energy in the winding is dissipated at zero voltage, the current fluctuations are smaller, hence the generated torque is slightly varying. This method is not suitable for control at high speeds as the phase current diminishes relatively slowly and in some machines this can lead to a negative torque production. As additional drawback it can be considered the low torque at low speeds and the poor dynamics of frequent reversals. On the other hand, in soft-chopping mode, the switching losses are lower and hence the energy efficiency is higher. This is good for the load in the aspect of temperature. In this switching mode it is possible to use different types of transistors for the upper and lower part of the bridge since one of them switches relatively less often, so it can be slower and in smaller package.

If the current and the voltage on the power switch have significant values at the same time, the dissipated power by that switch will also have a significant value. This mode is known as hard-chopping mode and is characterized by a full voltage drop on the power switch. In hard-chopping mode all the transistors in the circuit are actively switched. In this mode, the switching losses are significant, which results in efficiency reduction. The increase in the operating frequency is limited as the switches have certain heat dissipation capabilities. In addition, the conversion device is a source of electromagnetic interference. This is a heavy operating mode in temperature aspect. On the other hand, this is the only way to achieve a static torque at zero speed. In this mode, the speed and the direction both depend on the PWM duty cycle, which is the same for each pair of transistors - T1-T3 or T2-T4. In case of a motor it will rotate in positive direction when the duty cycle is greater than 50% and it will rotate in negative direction when it is less than 50%. With a duty cycle of 50% the current in both directions has same value and symmetrical duration so the motor is stopped. One main peculiarity of this circuit is that a shoot-through can emerge if the transistors T1 and T2 or T3 and T4 remain switched on at the same time. Such a situation can occur if T2 is turned on before T1 cuts off and this can happen because of the recovery time of each transistor which prevents it to be cut off instantaneously. To ensure proper operation, the bridge shoot through should always be avoided. This necessitates the introduction of the so called "interlock delay time" or "dead time" into the control scheme. It represents a short period that ensures some time for the corresponding power switch to be fully turned off. The dead time have to be selected so that to completely avoid the shoot-through in the inverter and on the other hand to be small enough so as not to interfere with the inverter's operation. A formula for calculating the dead time is given in [2] (1):

$$t_{dt} = \left[\left(t_{D\_OFF\_MAX} - t_{D\_ON\_MIN}\right) + \left(t_{PDD\_MAX} - t_{PDD\_MIN}\right)\right].1.2 \qquad (1)$$

In the above equation $t_{D\_ON\_MIN}$ and $t_{D\_OFF\_MAX}$ are the minimum and maximum on-delay time, and the t_{PDD_MIN} and t_{PDD_MAX} are the minimum and the maximum signal propagation times (delay) of the driver circuit. Finally, the result is multiplied by 1.2, which is a coefficient for certain security factor. The first difference in the equation derives from the parameters of the power switch itself and can be obtained from the datasheet of the transistor, and the second difference is typical for the control circuit and it can be obtained from the driver datasheet. In most cases, it is sufficient to know only Turn-On Delay Time and Turn-Off Delay Time of the transistor. The period of the dead time is typically in the order of 0.3 to 5us [2, 6, 15, 16, 19].
There exist several solutions to address the problem and all of them are based on implementing a mechanism for Dead Time Insertion (DTI).

This can be done in one of the following ways:
1. Using a delay circuits comprising of a resistor in parallel with a diode, feeding a capacitor. This method is not very precise due to the thermal dependence and the tolerances of the components.
2. Using a digital delay circuit which in fact represents a monostable multivibrator that introduces some delay cycles in the signal path [10].
3. Some microcontrollers have an integrated DTI unit which can be configured by registers [3, 4, 5].
4. There exist some specialized DTI integrated gate driver circuits like IX21844 by Ixys with programmable dead time of about 0.4-5us [6].
5. Of course it is almost always possible to insert a dead time using timers and comparators of a general purpose MCU if being careful about the timing. The drawback of this method is that the timer modules get rapidly exhausted thus making a multichannel PWM converter not possible to be implemented on a single device.

A summarizing comparison between hard-chopping and soft-chopping strategies is made in [12] and it is given in Table 1 below.

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table I comparison between hard and soft switching

Parameter	Hard Switching	Soft Switching
Switching loss	Severe	Low
Overall efficiency	Reduced	High
Heat-sink requirement	Normal	Low
Overall power density	Normal	High
EMI problem	Severe	Low
dv/dt problem	Severe	Low
Modulation scheme	Versatile	Limited

II. CONTROLLER DESIGN

A possible implementation solution for a fully digital PWM controller is given below. It employs the classical approach of PWM generation, i.e. without dead-time insertion – therefore this circuit is mostly suitable for soft-chopping switching. The block diagram of the device is shown in Fig. 2.

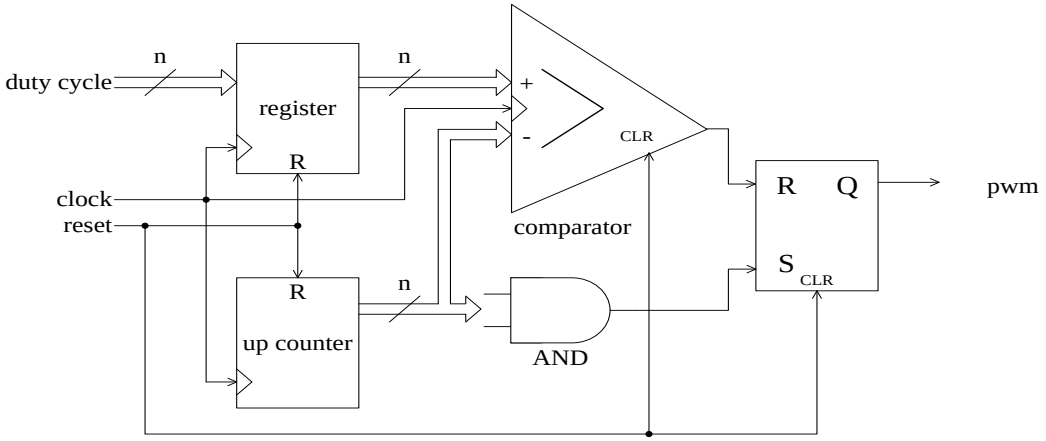

Fig. 2. Block diagram of a classical PWM modulator

The working principle of the circuit is based on using a counter and a comparator. When applying a reset signal the input register, the counter, the comparator and the output RS flip-flop all set their outputs to zero. After releasing the reset signal the duty cycle assignment is stored in the input register on the first rising clock edge and the value from the up-counter increments, i.e. it starts counting. The counter value is being compared by the comparator module to the value of the duty cycle and on equality the latter resets the output RS flip-flop. This flip-flop switches to logical 1 when all 2^n bits in the counter value are set to 1. This leads to issuing the rising edge of the PWM output. On the next rising edge of the clock signal the counter overflows and starts counting from 0 again. The comparator module compares the values of the duty cycle and the counter and resets the output flip-flop thus generating the falling edge of the PWM. This process repeats all over again. The bit-width of the PWM can be determined by the required precision and the working frequency of the modulator using equation (2).

$$n = \log_2 s \qquad (2)$$

, where s denotes the step count.

For example if the required frequency is f=2kHz (T=500us) and the resolution is of 512 steps, the bit count equals 9. After dividing the time period to the steps count, it can be obtained the period of a single step. In the example case it is 0.976us. This leads to a working frequency of the clock of 1.0246MHz. A standard frequency of 1MHz can be selected because the error of 2.46% is acceptably small.

A sample simulation waveform of the algorithm is depicted in Fig. 3.

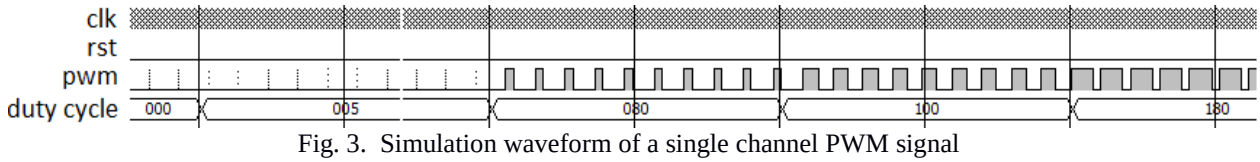

Fig. 3. Simulation waveform of a single channel PWM signal

The discussed algorithm can be improved by introducing delay logic and obtaining a dead time insertion (DTI). A block diagram of the device is shown in Fig. 4.

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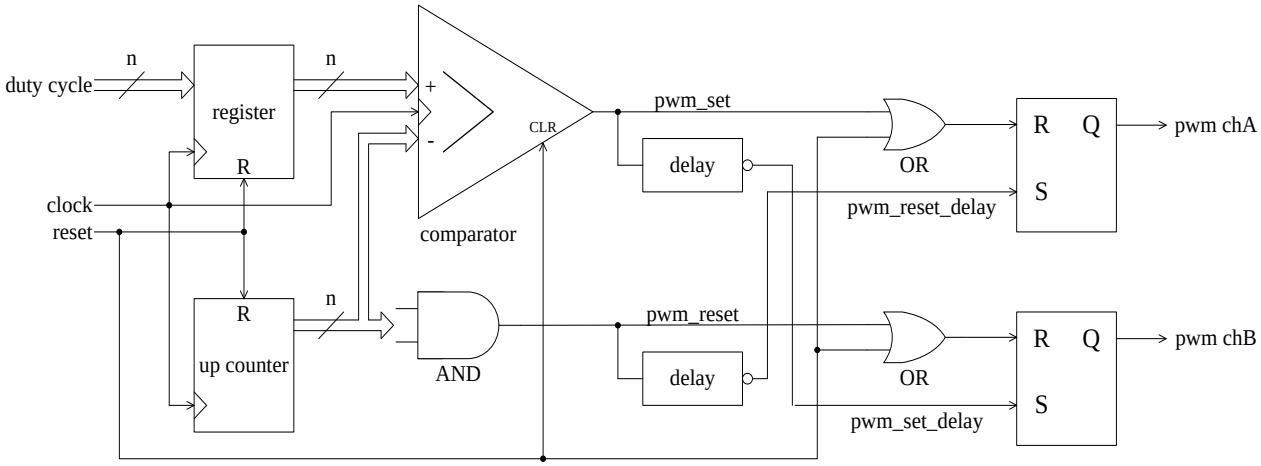

Fig. 4. Introducing Dead Time Insertion (DTI) to the PWM algorithm for two-channels topology

As it is seen from the figure the comparator and the AND gate no longer affect directly the RS flip-flop inputs but they affect two output RS flip-flops instead. This is done through a delay and OR logic which introduce the dead time. This circuit is suitable for full H-bridge control.

The delay block is implemented as a configurable monostable multivibrator [9, 10] which output is negated. The delayed reset signal from the AND gate (pwm_reset_delay) serves for setting the output RS flip-flop of channel A of the modulator. In the same time the delayed set signal from the comparator (pwm_set_delay) resets the output RS flip-flop of channel B. Introducing such a delay block gives opportunity for precise tuning of the dead time duration. If the PWM frequency is to be of greater value the delay multivibrator can be replaced with a simple counter which is capable of counting more clock cycles. It is natural to suppose that the duty cycle of such PWM modulator will be limited at both ends by the interlock delay time so that it becomes very important the duty cycle value to be no less than the dead time value. Violating this requirement will lead both channels to overlap meaning they will be active at the same time. That is why it is highly recommended to put additional limiting comparator circuitry before the duty cycle register.
The working principle of the modified PWM is illustrated in Fig. 5.

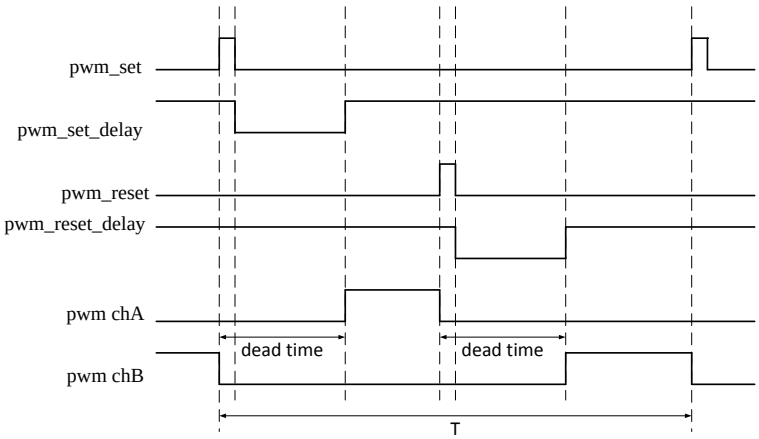

Fig. 5. Working principle of the modified PWM

The four control signals (pwm_set, pwm_set_delay, pwm_reset, pwm_reset_delay) are shown for clarity. The lower two rows visualize the two channels of the PWM module.

III. SIMULATION RESULTS AND EXPERIMENTAL WORK

The digital design of the PWM module is implemented on a Xilinx Spartan 3 FPGA device [23] and is written in Verilog HDL [7, 8, 9]. The simulation is performed in Xilinx ISim simulator. Simulation results are shown in Fig. 6 where some important internal signals are added – these are pwm_set, pwm_set_delay, pwm_reset and pwm_reset_delay. An enlarged area of the same waveform is shown in Fig. 7 giving a clear view of the dead time.

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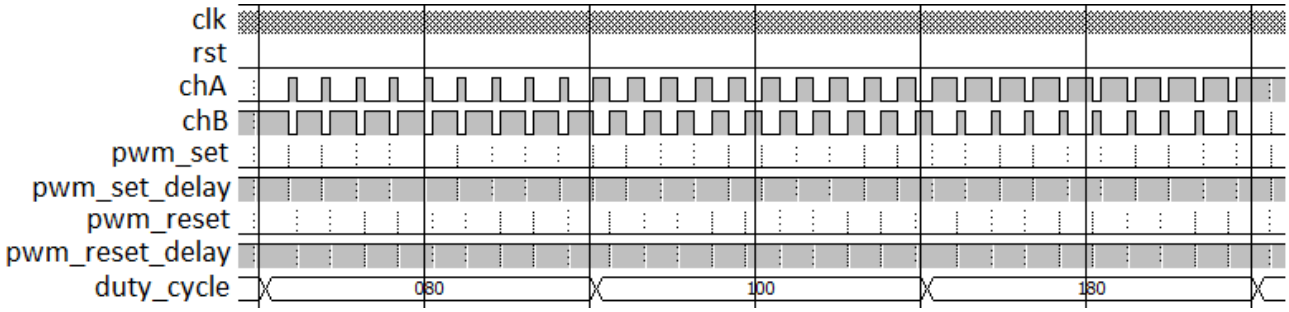

Fig. 6. Simulation waveform of a two channel PWM module with dead time control

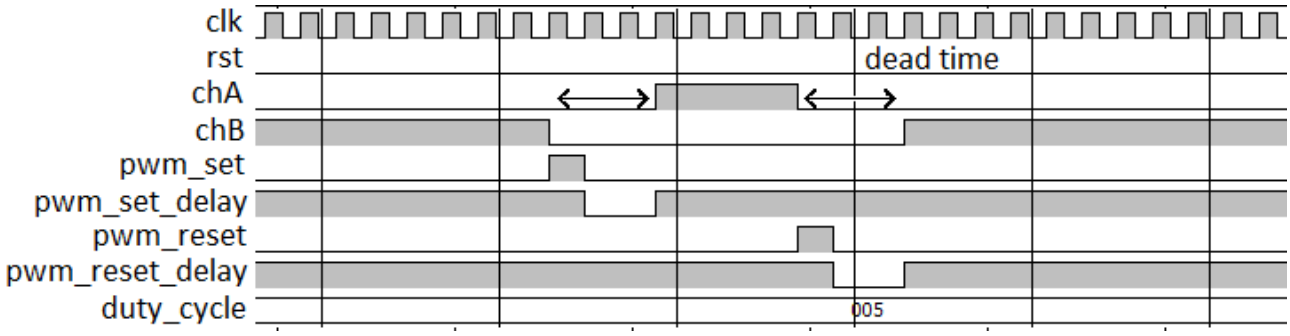

Fig. 7. Enlarged area of the simulation waveform of a two channel PWM module with dead time control

Experimentally obtained waveforms of an 8-bit PWM with clock frequency of 100kHz are shown in Fig. 8. The time resolution is 10us and the frequency of the PWM is about 390Hz. The usage of a programmable logic device permits the resolution to be configured to almost any value such as 9, 13 or 24 bits if needed. Also the clock frequency can be augmented in the order of tens to thousands MHz. In the figure it can be easily seen the dead time which is 30us for the sake of the experiment.

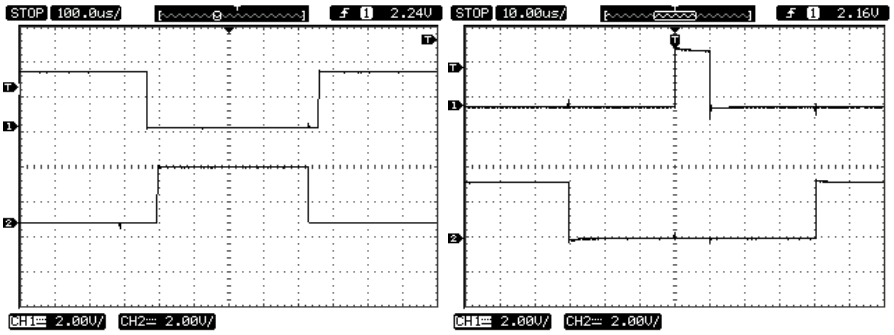

Fig. 8. Oscilloscope waveform of channels A and B for an 8-bit PWM at 100kHz clock with duty cycle of 0xD0 (left) and 0x02 (right)

The elaborated PWM module can be easily modified to support multiple parallel running channels. The setup is depicted in Fig. 9. As it can be seen the up-counter and the AND gate are common to all channels so they are instantiated once for the entire device. The duty cycle register, the comparator and the delay logic are repeated for every channel. The clock signal can be split into a low-frequency clock for the counter and a high-speed one for the duty cycle register which can further simplify routing. The number of channels depends on the available resources on the die of the selected chip and does not affect the performance of the module as the FPGA makes them run in parallel.

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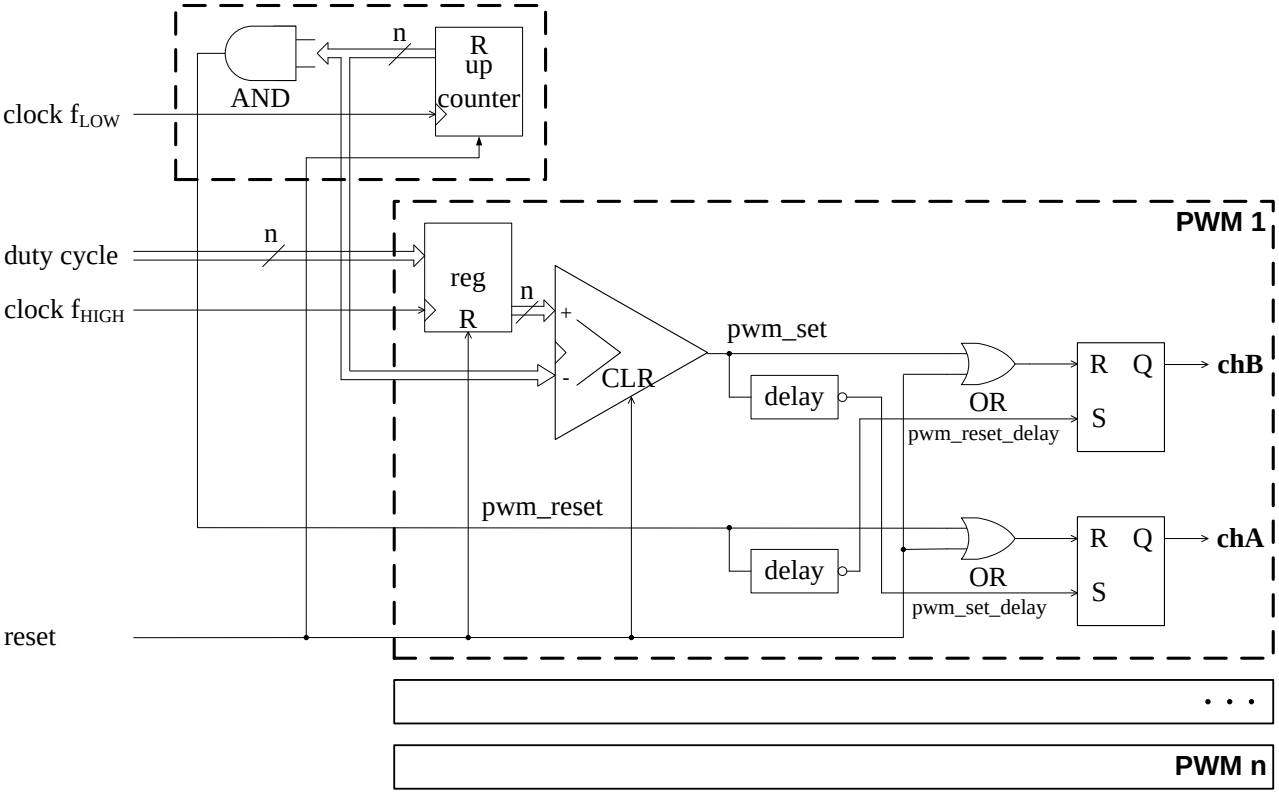

Fig. 9. Multichannel PWM configuration

The usage of FPGA device resources increments linearly with the increase of channels count that makes the design flow quite predictable. Brief device implementation statistics are shown in Fig. 10.

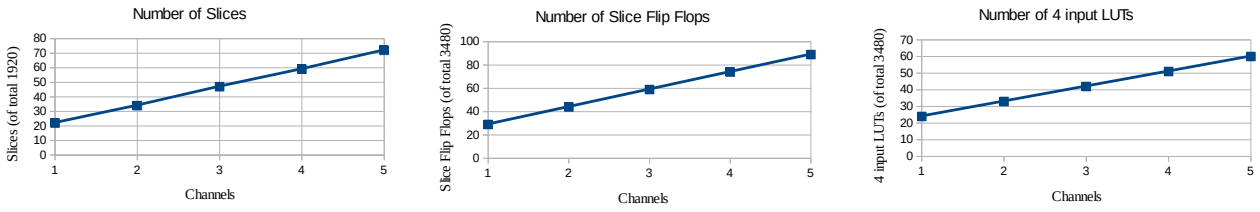

Fig. 10. Device resources utilization statistics for Xilinx Spartan-3 3S200FT256-4 FPGA

IV. CONCLUSION

Industrial systems for motor control are a rapidly developing sector which demand utmost performance from not only the power devices but also from the computational units. There is a constantly rising demand for fast and complex control algorithms which often require parallel execution. That is why the overall tendency is towards implementing strictly digital control devices. In this area conventional microcontrollers still take a major place but their usage is more and more frequently replaced by programmable logic devices. The reason is quite obvious – they are inherently capable of executing parallel running algorithms which makes them outperform the speed of most if not even all microcontrollers available on the market. In this research an advantageous multichannel PWM controller with embedded dead time is discussed. It is implemented on a Spartan-3 FPGA device but its design can be easily ported to any other programmable logic family not excluding the low cost CPLD circuits. Moreover the design is quite versatile and gives opportunity to expand the number of channels depending only on the available FPGA resources. This makes the proposed controller useful in a broad area of industrial applications such as multi-axis computer numeric control machines or complex robotics systems.

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